

ETHERNET APPLICATION EXAMPLE

Involving Marvell Alaska 88E1512

Integrated 10/100 Mbps Energy Efficient Ethernet Transceiver

Overview

Piksi Multi can provide a 10/100 Ethernet port for network connections. This article describes how to use a **Marvell Alaska 88E1512** Ethernet PHY with Piksi Multi at a hardware level to enable this interface.

In the reference design, the recommended Marvell part operates at **3V3** and connects to the Zynq-7020 AP System on a Chip (SoC) through Piksi Multi's high density connector 1 (HDC1). The PHY is connected to the Zynq MIO Bank 1/501 (1V8) via the Reduced Gigabit Media Independent Interface (RGMII).

The 88E1512 also requires a **25 MHz** input clock. A **Discera DSC1001DI1-025.0000** is used in this reference design. The RJ-45 used has status LED's and magnetics built-in.

After power-up the PHY starts with Auto Negotiation enabled, advertising 10/100 link speeds and full duplex.

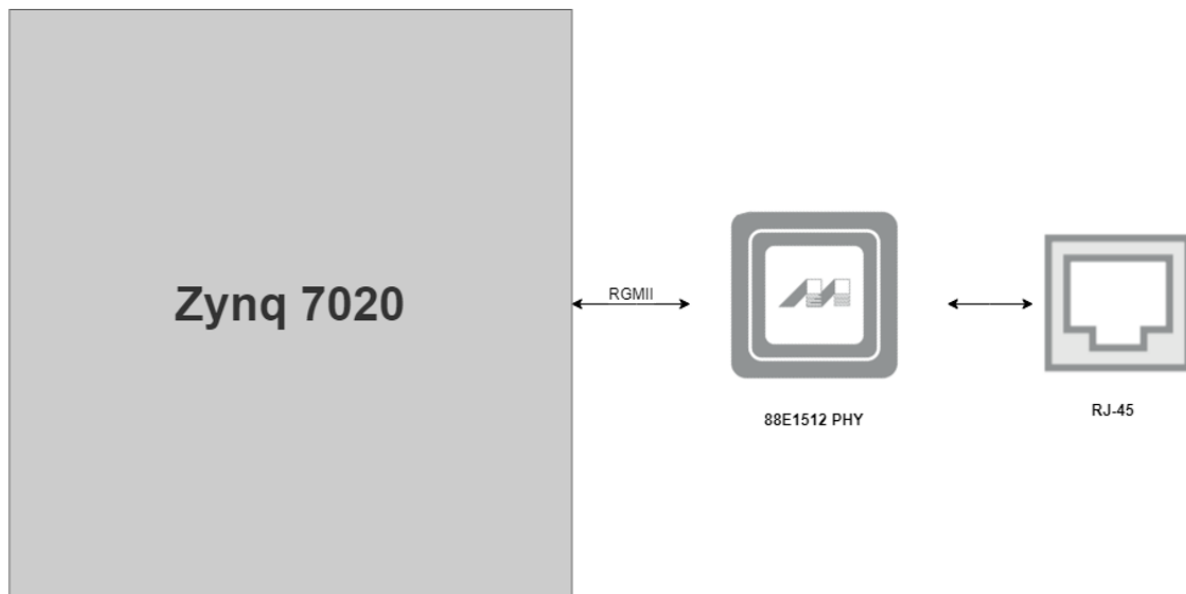


Fig 1. Alaska 88E1512 high level application

Signal Name	Description	Zynq pin	Piksi HDC 1 Pin	88E1512 pin
RX_CLK	Receive Clock	B17	14	46
RX_CTRL	Receive Control	D13	24	43
RXD[3:0]	Receive Data	RXD0: D11 RXD1: A16 RXD2: F15 RXD3: A15	16	44 45 47 48
TX_CLK	Transmit Clock	A19	18	53
TX_CTRL	Transmit Control	F14	20	56
TXD[3:0]	Transmit Data	TXD0: E14 TXD1: B18 TXD2: F15 TXD3: A17	22	50 51 54 55
MDIO	Management Data	C11	13	8
MDC	Management Clock	C10	23	7
ETH_RST_N**	PHY Reset	E6	32	16
3V3	To be generated by the customer	-	-	20 25 36
E_1V8	Generated by the Ethernet PHY chip	-	-	3 10 11 19 26 35 38 39 49 52
E_1V0	Generated by the Ethernet PHY chip	-	-	6 40 42

Table 1. Ethernet PHY pin assignment and definitions

** PHY Reset is handled by Piksi Multi, so no need to add an external resistor.

Status LED

Status indicator LEDs are on RJ45 connector that indicate traffic and valid link state.

Function	Description
LINK	Link 10/100
ACTIVITY	Transmitting (or) Receiving

Table 2. RJ45 LED status

Power supply requirement when using internal regulators

Marvell Alaska 88E1512 Ethernet PHY can be supplied with a single 3V3 supply. Please choose a supply based on the below data.

Functional Description	AVDD33	AVDDC18/AVDD18	DVDD	Setup
Supply source	3V3	E_1V8 from internal regulator	E_1V0 from internal regulator	Single 3.3V external supply Internal regulator enabled

Table 3. Power supply options - Integrated Switching Regulator (REG_IN)

Symbol	Parameter	Pins	Condition	Typical	Units
I_{REG_IN}	3V3 Internal Regulator Supply	REG_IN	RGMII over 1000BASE-T with traffic	80	mA
			RGMII over 100BASE-TX with traffic	32	mA
			RGMII over 10BASE-T with traffic	22	mA
I_{REG_IN}	3V3 Internal Regulator Supply	REG_IN	SGMII over 1000BASE-T with traffic	92	mA
			SGMII over 100BASE-TX with traffic	53	mA
			SGMII over 10BASE-T with traffic	43	mA
			RGMII over 1000BASE-X	28	mA
			RGMII over SGMII at 1000 Mbps	28	mA
			RGMII over SGMII at 100 Mbps	27	mA
			RGMII over SGMII at 10 Mbps	26	mA
			Energy Detect	25	mA
			IEEE Power Down	13	mA

Table 4. Current consumption REG_IN

PCB layout considerations

- The ideal Ethernet differential impedance between the MDI0±, MDI1±, MDI2±, and MDI3± traces (between MDI0+ and MDI0-, MDI1+ and MDI1-, MDI2+ and MDI2-, MDI3+ and MDI3-) should be 100 Ohm. The Ethernet differential impedance between the MDI0+/ MDI0-/MDI1+/ MDI1- MDI2+/MDI2/ MDI3+/ MDI3- trace and GND should be 50 Ohm respectively. The designer can use the trace width of MDI0+/ MDI0-/ MDI1+/ MDI1- MDI2+/MDI2/ MDI3+/ MDI3- traces to fine tune the Ethernet differential impedance value (a wider trace has a smaller impedance value).
- The crystal/oscillator clock source and the switching noises from digital signals should be kept away from the MDI0±, MDI1±, MDI2±, and MDI3± differential pairs. Moreover, the crystal/oscillator may be sensitive to wander capacitances and noise from other signals; it is better to deploy the crystal far away from I/O ports, high frequency signal traces, magnetic, board edges, and so on.
- The MDI0±, MDI1±, MDI2±, and MDI3± differential pairs should be routed as close as possible. The trace spacing D1 between MDI0+ and MDI0- (or between MDI1+ and MDI1-, MDI2+ and MDI2-, MDI3+ and MDI3-) pair should be in 6 ~ 8 mils. The trace width should be adjusted accordingly to yield the required trace impedance.

- The spacing D2 should be larger than 200 mils. If the PCB layout is difficult to meet this requirement, the D2 spacing should be as larger as possible.
- Route the MDI0±, MDI1±, MDI2±, and MDI3± differential pairs as straight as possible and keep them in parallel for differential pairs.
- Keep the trace length difference between MDI0+ and MDI0- (or between MDI1+ and MDI1-, MDI2+ and MDI2-, MDI3+ and MDI3-) pair within 700 mils.
- Route the MDI0±, MDI1±, MDI2±, and MDI3± differential pairs running symmetric, equal length and close whenever possible.
- Avoid using vias on the traces of the MDI0±, MDI1±, MDI2±, and MDI3± differential pairs. If the PCB layout really needs to use vias on the differential pairs, please match the vias to keep the differential pairs balanced.
- Uncontrolled impedance runs and stubs should be kept to minimum.
- Avoid routing the signal trace with right angle, instead, the signal trace should be routed with multiple 135° angles.
- The RJ-45 is recommended to have metal shielding that connects to chassis ground to reduce EMI emission.
- The isolated side should have the chassis ground "island" placed. The MDI pairs are placed above a continuous chassis ground plane.
- Ensure that the power supply is well regulated (3.3 V DC ±5%).

References

Document	Provider	Notes
Marvell Alaska 88E1512 datasheet	Marvell	
Xilinx Technical Reference Manual	Xilinx	Useful in understanding Gigabit Ethernet MAC and Xilinx design recommendations
Piksi-Multi-Ethernet-Interface-design-files.zip	Swift	All design files to support application - Bill of Materials - Altium design files